Vol. 4.Special Issue ICCSII ISSN 2079-8407
Journal of Emerging Trends in Computing and Information Sciences

http://www.cisjournal.org

# Circuit Proposition for Copying the Value of a Resistor into a Memristive Device Supported by HSPICE Simulation

**[1]Farshad Merrikh-Bayat, [2] Nafiseh Mirebrahimi, [3] Farnood Merrikh-Bayat**

[1]Assistant Prof., Department of Electrical and Computer Engineering, University of Zanjan, Zanjan, Iran

[2]MSc student, Department of Electrical and Computer Engineering, University of Zanjan, Zanjan, Iran

[3]PhD, ECE Department, University of California Santa Barbara, US

E-mail: [1]f.bayat@znu.ac.ir, [2]nafisehmirebrahimi@yahoo.com, [3]farnoodmb@ece.ucsb.edu

## ABSTRACT

Memristor is the fourth fundamental passive circuit element with potential applications in development of analog memories, artificial brains (with the capacity of hardware training) and neuro-science. In most of these applications the memristance of the device should be set to the desired value, which is currently performed by trial and error. The aim of this paper is to propose a circuit for copying the value of a given resistor into a memristive device. HSPICE simulations are also presented to confirm the efficiency of the proposed circuit.

**Keywords:** *memristance auto tuning, memristor, HSPICE simulation, Op-Amp, nonlinear circuit*

## 1. INTRODUCTION

On 1 May 2008 a research group in Hewlett-Packard Labs reported the physical realization of the first memristor [1], the fourth fundamental passive circuit element, which was already predicted by Leon Chua in 1971 [2]. After that innovation, many researchers seek the applications of memristor in variety of scientific fields such as neuroscience, neural networks and artificial intelligence. It is now clear that this passive circuit element can have many applications in, for instance, development of analog neural networks and emulation of human learning [3], building programmable analog circuits [4], [5], constructing hardware for soft computing tools [6], implementing digital circuits [7], second and higher harmonics generation [8], and in the field of signal processing [9], [10].

One main reason for this great interest to memristive systems is that these systems have a high potential to overcome most of the challenges in front of today's digital systems. For example, it is proved that these systems can be constructed much denser than their counterparts through the use of nano-crossbar technology, and moreover, they consume a considerably less energy [11].

Roughly speaking, memristor can be considered as a simple resistor whose resistance is changed by applying voltage or current to it. This means that an analog value can be stored in this kind of device by setting its resistance equal to the desired value. It concludes the fact that memristors can play the role of analog memories in analog circuits since they can hold their resistance unchanged until a voltage or a current is applied to them. However, there is a challenge in front of using memristors as analog memories. The problem is that we need a simple and effective circuit for accurate tuning the resistance of the given memristor to the desired value. This problem has been partly studied by authors of this paper and the results are presented in [12]. In that study a circuit for storing an analog voltage signal in a memristor was proposed. The aim of this paper is to propose a circuit for automatic adjustment of the resistance of a memristor to the value of a given resistor.

The rest of this paper is organized as follows. In Section 2 we briefly review the notion of memristive systems. Section 3 is devoted to the HSPICE model of the HP-memristor used in our simulations. Two electronic circuits for automatic tuning the resistance of HP-memristive to the desired value are proposed in Section 4. Results of some HSPICE simulations are also presented in this Section. Finally, Section 5 concludes the paper.

## 2. BRIEF REVIEW OF MEMRISTIVE SYSTEMS

A *memristive system* can be described by the equations:

$$v(t) = R(\mathbf{x}, i)\, i(t) \quad (1)$$

$$\frac{d\mathbf{x}}{dt} = f(\mathbf{x}, i) \quad (2)$$

where $\mathbf{x}$ is a vector representing internal state variables of system, $t$ is the time variable, $v(t)$ and $i(t)$ are the voltage and current across the device, respectively, and $R$ is a scaler called *memristance* [1], [13]-[15]. As it can be observed in (2), the time derivative of states of this system depends on the electrical current passing through it. For this reason this system is sometimes called the *current-controlled* memristive system.

*Current-controlled memristor* is a special case of current-controlled memristive systems. The most basic mathematical definition of a current-controlled memristor is given by the following equations [1]:

$$v = R(x)\, i \quad (3)$$

$$\frac{dx}{dt} = i \quad (4)$$

Hence, according to (1) and (2) the current-controlled memristor can be considered as a kind of (time-varying) resistor whose resistance depends on the history of the current passed through it and also to the internal state of device.

Figure 1 shows the symbol of memristor used in the literature. The memristor shown in this figure is an asymmetric device which has the property that applying positive voltage to the terminal denoted by the black thick line

with respect to other terminal decreases its resistance, and vice versa. It concludes that in practice the memristance of a memristor can be adjusted to the desired value by applying a suitable alternating-polarity voltage to it [16] (note that in practice the memristance of memristive devices always lies between two limiting values denoted as $R_{on}$ and $R_{off}$, where $R_{on} < R_{off}$ and the ratio of these two resistances is usually given as $10^2$-$10^3$). Since such an appropriate voltage generator is not available at this time, in practice the memristance of the given memristor is adjusted to the desired value by trial and error. More precisely, positive and negative voltages are applied to the memristor to decrease and increase its memristance respectively until it takes a value close to the desired one. The main drawback of this approach is that it is commonly time consuming, and moreover, the results may not be accurate enough.

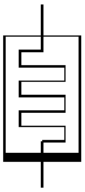

**Fig 1:** The symbol of memristor

In the following, we will propose a circuit for automatic and accurate tuning the memristance of the given memristor to the desired value in a reasonably short time. But before that we need to present the HSPICE model of the memristor constructed in HP labs since it will be used in our simulations.

## 3. HSPICE MODEL OF HP-MEMRISTOR

The HSPICE model of the memristor used in simulations of this paper is based on the physical model proposed for memristor in [1] (which is currently known as the HP-memristor) and the corresponding electrical model proposed for it in [14]. In the physical model proposed in [1], the memristor is considered as a two-layer thin film of $TiO_2$ as shown in Fig. 2 ($D \approx 10\text{nm}$), which is sandwiched between two platinum contacts. One of the layers in this figure is doped with oxygen vacancies (and consequently, behaves as a semiconductor) and the other is undoped (and consequently, behaves an insulator). The boundary between two layers is moved in the same direction as the electrical current passes. It is concluded from Fig. 2 that the total resistance of the memristor, $R_{mem}(x)$, is equal to the sum of the resistances of doped and undoped regions as follows:

$$R_{mem}(x) = R_{on}x + R_{off}(1-x) = R_{off} - (R_{off} - R_{on})x \quad (5)$$

where

$$x = \frac{w}{D} \in (0,1) \quad (6)$$

and $R_{off}$ and $R_{on}$ (which correspond to $w = 0$ and $w = D$, respectively) are equal to the maximum and minimum possible values for the resistance of memristor, respectively. In fact, as mentioned before, the resistance of the memristor is always between the limiting values $R_{on}$ and $R_{off}$.

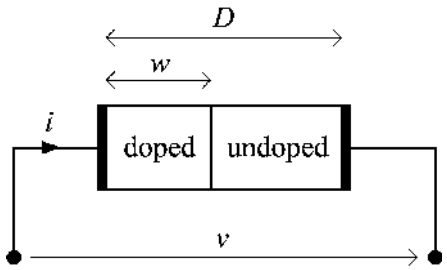


**Fig 2:** The physical model of memristor

According to the discussions presented in [1] and [14] the derivative of $x$ with respect to time can be considered as the following:

$$\frac{dx}{dt} = ki(t)f(x), \qquad k = \frac{\mu_v R_{on}}{D^2} \quad (7)$$

where $\mu_v \approx 10^{-14}\,\text{m}^2\text{s}^{-1}\text{V}^{-1}$ and $f(x)$ is the so-called *window function*. The window function $f(x)$ in (7) can be defined in many different ways. One possible approach is to define it as [14], [17]:

$$f(x) = 1 - (2x-1)^p \quad (8)$$

where $p$ is a positive integer.

Based on the above discussions and the approach proposed in [14] for electrical modeling of memristive devices, the HSPICE model presented in Table 1 is used in simulations of this paper (this model is the same as the one proposed in [14] with small modifications to make it compatible with HSPICE simulator). In this table, which approximately models the HP-memristor, it is assumed that $R_{on} = 100\Omega$, $R_{on} = 16\,\text{k}\Omega$, $p = 10$, and the memristance of the device is initially equal to $1\,\text{k}\Omega$.

**Table 1:** HSPICE model of the HP-memristor used in simulations of this paper (the fifth line of this code is the continuation of fourth line and during the simulation these two lines should be typed in a same line).

```
******** HP memristor model ********
.SUBCKT memristor Plus Minus
+ Ron=100 Roff=16K Rinit=1K D=10N uv=10F p=10
Gx 0 x CUR='(I(Emem)*(uv*Ron))/(pow(D,2))*(1-
pow((2*V(x)-1),(2*p)))'
Cx x 0 1 IC='(Roff-Rinit)/(Roff-Ron)'
Raux x 0 1T
Emem plus aux VOL='-I(Emem)*V(x)*(Roff-Ron)'
Roff aux minus 'Roff'
.ENDSs
```

## 4. PROPOSED CIRCUIT FOR COPYING THE RESISTANCE OF THE GIVEN RESISTOR INTO A MEMRISTOR

Figure 3 shows the proposed circuit for increasing the resistance of the given memristor from $R_{mem}$ to the desired value $R_{ref}$ ($R_{ref} > R_{mem}$). More precisely, in this figure it is assumed that the initial value of memristor is smaller than $R_{ref}$ and we want the circuit to increase the resistance of the memristor to the desired value $R_{ref}$. In Fig. 3 the value of $R_1$

must be considered equal to $R_2$ and theoretically, they can be considered equal to any number. Any Op-Amp can also be used in this connection. All simulations of this paper are performed assuming $R_1 = R_2 = 1\text{k}\Omega$, when the AD711a Op-Amp is applied and *A*=5V.

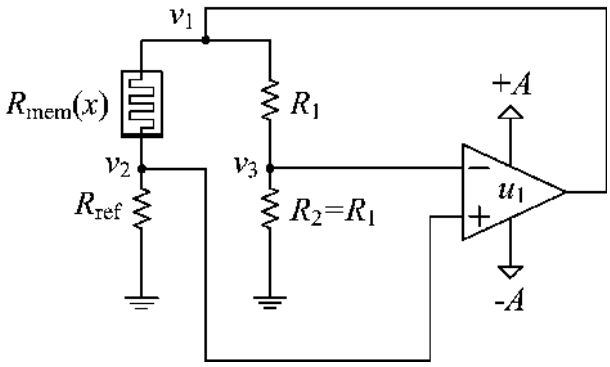


**Fig 3:** The proposed circuit for increasing the resistance of memristor from $R_{mem}$ to $R_{ref}$.

Analysis of the circuit shown in Fig. 3 is straightforward. Considering the fact that $R_1 = R_2$, we always have $v_3 = v_1 / 2$. On the other hand, since at the beginning we have $R_{ref} > R_{mem}$, and consequently $v_2 > v_1 / 2$, the output of Op-Amp is at the high state, which leads to increasing the resistance of memristor. By increasing the resistance of memristor, $v_2$ is also increased which results in decreasing the output voltage of Op-Amp. Consequently, at steady state we have $v_2 = v_3$, $v_1 = 0$, and $R_{mem} = R_{ref}$.

Figures 4-6 show the HSPICE simulations of the circuit shown in Fig. 3. All of these simulations are done in the time range 0-15ms, where the time step is considered equal to 1ns. Note that larger time steps may result in inaccurate results or even divergence of the solutions. Another point that should be noted during simulation is that the port of memristor with plus sign in Table 1 corresponds to the port with black thick line in Fig. 3. Figure 4 shows the resistance of the memristor of Fig. 3 versus time. As it can be observed, the memristance of the device tends to $R_{ref} = 2\text{k}\Omega$ as the time is increased. A small steady-state error observed in Fig. 4 may because of the value considered for time step since this error is decreased by decreasing the time step used for simulation. In this simulation the memristance reaches its steady-state value after about 7ms. Simulations show that this time is increased by increasing $R_{ref}$ or decreasing the power supply applied to Op-Amp (i.e., the value of *A* in Fig. 3). For example, Fig. 7 shows the resistance of the memristor of Fig. 3 versus time when $R_{ref} = 4\text{k}\Omega$. This figure clearly shows that increasing $R_{ref}$ from $2\text{k}\Omega$ to $4\text{k}\Omega$ increases the settling time of the system response from 7ns to 40ns.

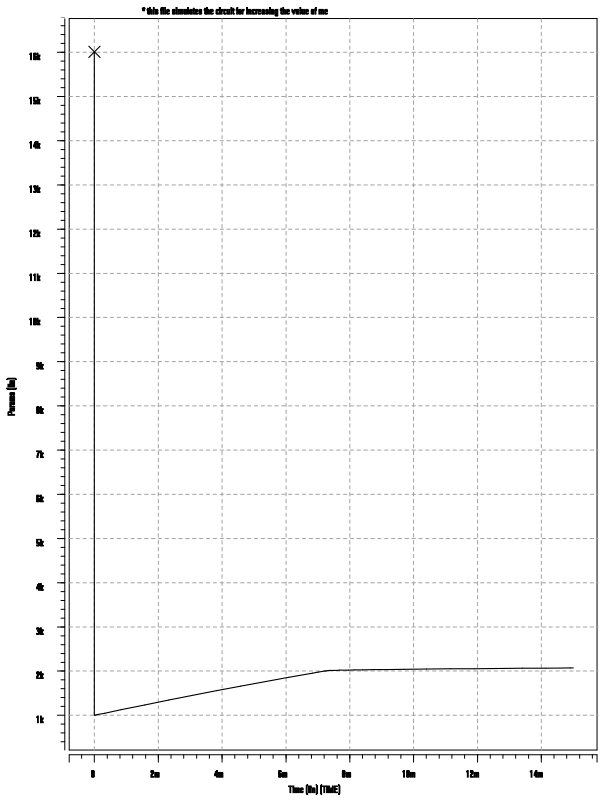

**Fig 4:** Resistance of the memristor of Fig. 3 versus time when $R_{ref} = 2\text{k}\Omega$ and the initial value of memristor is equal to $1\text{k}\Omega$. Memristance of the device tends to $R_{ref}$ by increasing the time.

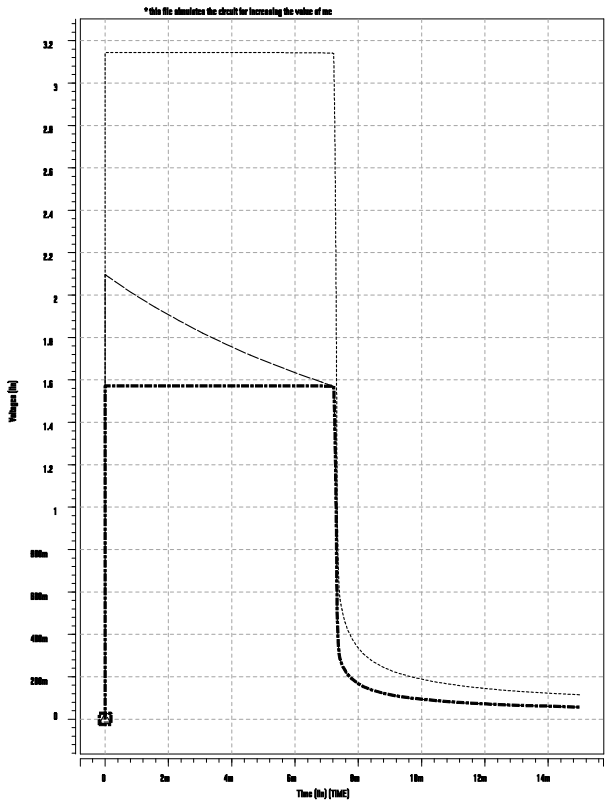

**Fig 5:** The plot of $v_1$ (dotted curve), $v_2$ (dashed curve), and $v_3$ (dashed-dotted curve) in Fig. 3 versus time ( $R_1 = R_2 = 1\text{k}\Omega$ , $R_{ref} = 2\text{k}\Omega$ , and $A$=5V).

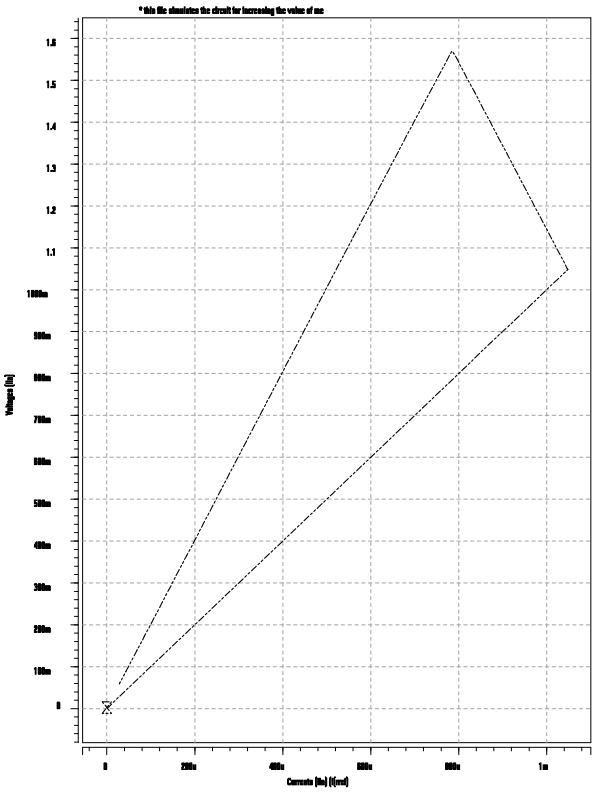

**Fig 6:** Plot of the voltage across memristor versus the current passes through it in Fig. 3 ( $R_1 = R_2 = 1\text{k}\Omega$ , $R_{ref} = 2\text{k}\Omega$ , and $A$=5V). The slope of plot at any point indicates the memristance of device at that point.

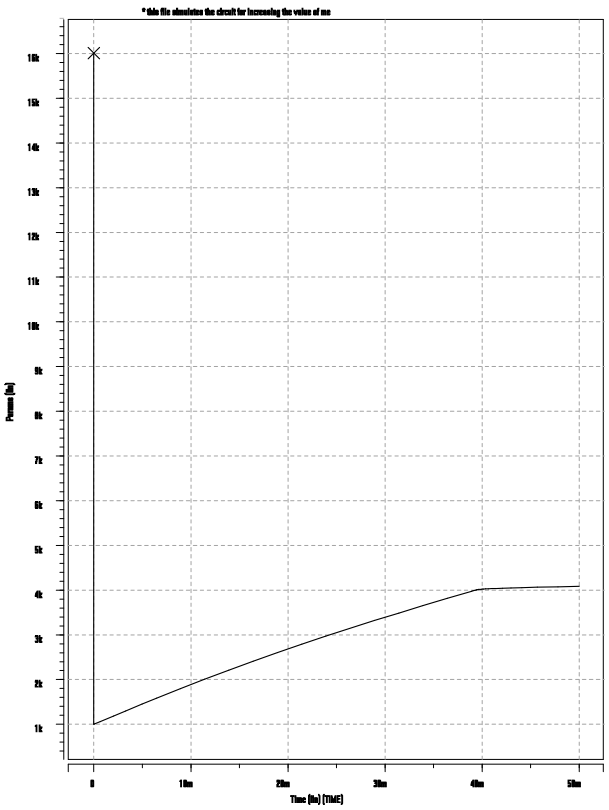

**Fig 7:** Resistance of the memristor of Fig. 3 versus time when $R_{ref} = 4\text{k}\Omega$ and the initial value of memristor is equal to $1\text{k}\Omega$.

It can be easily verified that the circuit shown in Fig. 3 does not work when $R_{ref} < R_{mem}$, that is, this circuit cannot be used for decreasing the memristance of the given memristive device. In such cases the circuit shown in Fig. 8 can be used instead. The function of this circuit can be explained similar to the circuit shown in Fig. 3 (note to the similarities between these two circuits).

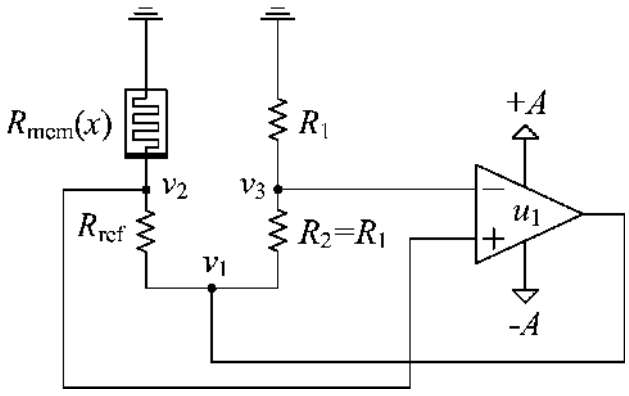


**Fig 8:** The proposed circuit for decreasing the resistance of memristor from $R_{mem}$ to $R_{ref}$.

Figures 9-11 show the simulation results of the circuit shown in Fig. 8. Similar to the previous simulations these results are also obtained assuming $R_1 = R_2 = 1\text{k}\Omega$, $A$=5V, and the time step of 1ns, while it is assumed that $R_{ref} = 500\Omega$ and the resistance of memristor is initially equal to $2\text{k}\Omega$. Figure 9 clearly shows that the proposed connection can effectively decrease the memristance of the device until it becomes equal to the desired value $R_{ref}$. Figure 10 shows the voltage signals corresponding to the simulation of Fig. 9. As it can be observed in this figure, $v_2$ and $v_3$ become equal after less than 6ms. Figure 11 shows the plot of voltage across memristor in Fig. 8 versus the corresponding current pass through it. The slope of this curve at any point on it indicates the resistance of the memristor at that point. It can be easily concluded from this figure that the memristance of device tends to $500\Omega$ as the time is increased. Note that the differences between the simulation results presented in Figs. 6 and 11 are mainly because of two reasons: First, the memristor is an asymmetric device, and second, these two simulations are performed assuming different initial and final values.

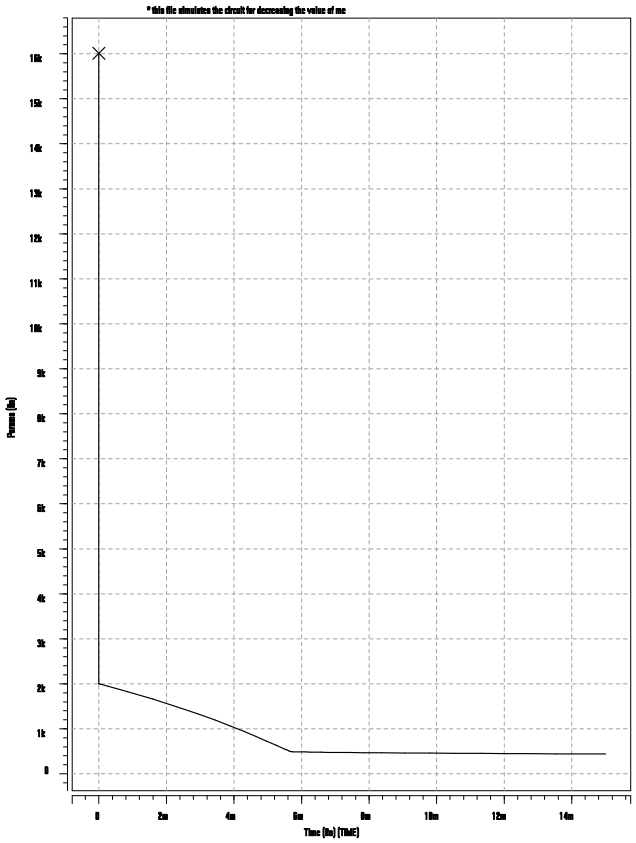

**Fig 9:** Resistance of the memristor of Fig. 8 versus time when $R_{ref} = 500\Omega$ and the initial value of memristor is equal to $2\text{k}\Omega$. Memristance of the device tends to $R_{ref}$ by increasing the time.

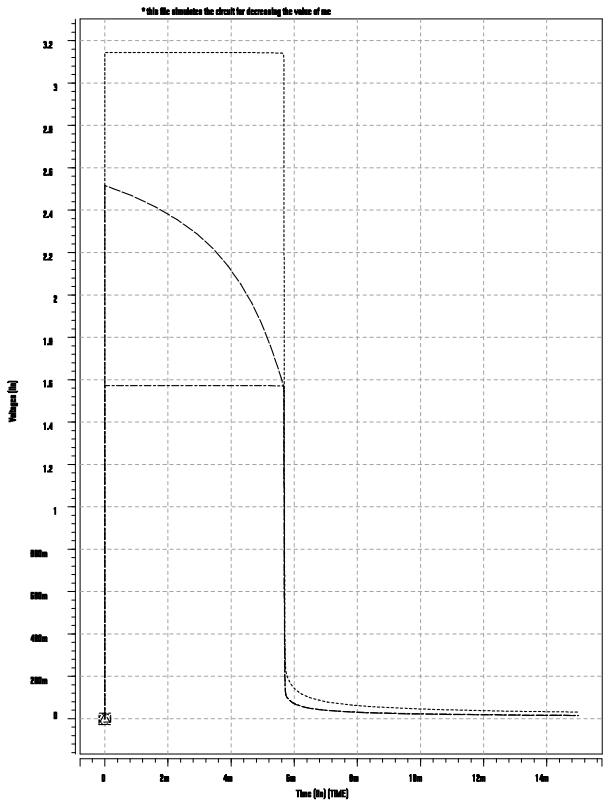

**Fig 10:** The plot of $v_1$ (dotted curve), $v_2$ (dashed curve), and $v_3$ (dashed-dotted curve) in Fig. 8 versus time ($R_1 = R_2 = 1\text{k}\Omega$, $R_{ref} = 500\Omega$, and $A$=5V).

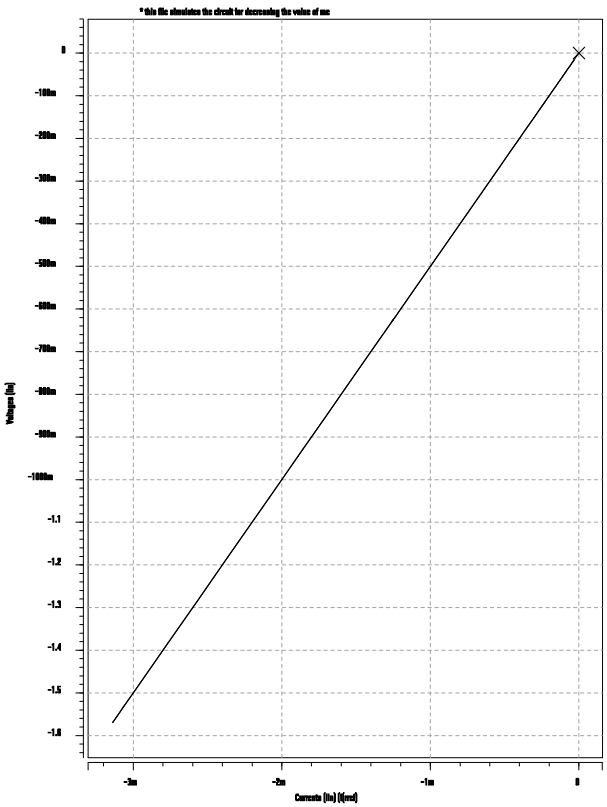

**Fig 11:** Plot of the voltage across memristor versus the current passes through it in Fig. 8 ($R_1 = R_2 = 1\text{k}\Omega$, $R_{ref} = 500\Omega$, and $A$=5V). The slope of plot at all points is approximately equal to 0.5, which corresponds to the resistance of $500\Omega$ for memristor, as it is expected.

## 5. DISCUSSION AND CONCLUSION

Two circuits for adjusting the resistance of a memristor to the value of the given resistor are proposed in this paper, and HSPICE simulations are presented. One of the proposed circuits can be used for increasing the memristance of the device to the desired value and the other one can be used for decreasing it. These circuits can be used for adjustment of the resistance of the given memristor to the desired value and copying the value of a resistor into it.

There are, however, many other questions that can be considered as the subject of future studies. Some of them are listed below:

- The proposed circuits can be implemented by using few transistors instead of applying an Op-Amp. In fact, there is no need to use an Op-Amp, which may consist of tens of transistors, in these circuits. More simple designs are desired and can be considered as the subject of future work.
- We proposed two circuits in this paper: one for increasing the memristance of the device and the other for decreasing it. In practice it is highly demanded to have a unique circuit with the ability of automatic adjustment of the memristance of the device to the desired value either by increasing or decreasing its resistance. Development of such a

circuit (possibly by combining the proposed two circuits) can be considered as the subject of future studies.

- Intuitively, it is expected that the proposed circuits can be used for automatic adjustment of the resistance of any memristive device (in addition to the HP-memristor studied in this paper). It is important to provide a mathematical proof for this statement and exactly determine the possible limitations of the proposed designs. It may even be observed that the application of proposed circuits is limited to a certain class of memristive devices. Since the circuits studied in this paper are nonlinear in nature, the Lyapunov stability theorem [18] can be used for this purpose.
- All simulations of this paper are carried out assuming that the reference resistor is constant (i.e., it is not varied with time). Although it is expected that the proposed circuits can handle time-varying reference resistors, it needs mathematical proof and numerical simulation, which is not performed in this paper.
- Another very important issue is to design a simple circuit for copying the analog value stored in a memristive device (in the form of its resistance) into another memristor. Such a circuit is useful in dealing with analog memories implemented on crossbar structures.

## REFERENCES

[1] D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, “The Missing Memristor Found”, Nature, vol. 453, pp. 80-83, 1 May 2008.

[2] L.O. Chua, “Memristor-The Missing Circuit Element”, IEEE Trans. on Circuit Theory, vol. CT-18, no. 5, pp. 507-519, 1971.

[3] Y.V. Pershin, S. La Fontaine, M. Di Ventra, “Memristive Model of Amoeba's Learning”, Phys. Rev. E, vol. 80, pp. 021926/1-021926/6, 2009.

[4] Y.V. Pershin, M.D. Ventra, “Practical Approach to Programmable Analog Circuits with Memristors”, IEEE Transactions on Circuits and Systems I: Regular Paper, vol. 57, no. 8, pp. 1857-1864, 2010.

[5] F. Merrikh-Bayat, S.B. Shouraki, “Memristor-Based Circuits for Performing Basic Arithmetic Operations”, Procedia-Computer Science Journal, vol. 3, pp. 128-132, 2011.

[6] F. Merrikh-Bayat, S.B. Shouraki, “Memristor Crossbar-Based Hardware Implementation of IDS Method”, IEEE Transaction on Fuzzy Systems, vol. 19, no. 6, pp. 1083-1096, 2011.

[7] P. Kuekes, “Material Implication: Digital Logic with Memristors”, Proceedings of the Memristor and Memristive Systems Symposium, 21 November 2008.

[8] G.Z. Cohen, Y.V. Pershin, M. Di Ventra, “Second and Higher Harmonics Generation with Memristive Systems”, arXiv link: http://arxiv.org/abs/1202.4727

[9] B.L. Mouttet, “Proposal for Memristors in Signal Processing”, Proceedings of the Nano-Net Conference, vol. 3, pp. 11-13, Sept. 2008.

[10] F. Merrikh-Bayat, S.B. Shouraki, “Mixed Analog-Digital Crossbar-Based Hardware Implementation of Sign-Sign LMS Adaptive Filter”, Analog Integrated Circuits and Signal Processing, vol. 3, no. 1, pp. 41-48, 2011.

[11] G. Snider, R. Amerson, D. Carter, H. Abdalla, M.S. Qureshi, J. Leveille, M. Versace, H. Ames, S. Patrick, B. Chandler, A. Gorchetchnikov, E. Mingolla, “From Synapses to Circuitry: Using Memristive Memory to Explore the Electronic Brain”, IEEE Computer, vol. 44, no. 2, pp. 21-28, February 2011.

[12] F. Merrikh-Bayat, F. Merrikh-Bayat, N. Mirebrahimi, “A Method for Automatic Tuning the Memristance of Memristive Devices with the Capacity of Applying to Memristive Memories”, Proceedings of the IEEE International Conference on Computer Systems and Industrial Informatics, Dec. 18-20, 2012, Sharjah, UAE.

[13] M. Di Ventra, Y.V. Pershin, L.O. Chua, “Circuit Elements with Memory: Memristors, Memcapacitors, and Meminductors”, Proceedings of the IEEE, vol. 97, no. 10, pp. 1717-1724, 2009.

[14] D. Biolek, Z. Biolek, V. Biolkova, “SPICE Modeling of Memristive, Memcapacitative and Meminductive Systems”, Proceedings of the European Conference on Circuit Theory and Design - ECCTD, pp. 249-252, 2009.

[15] G.Z. Cohen, Y.V. Pershin, M. Di Ventra, “Lagrange Formalism of Memory Circuit Elements: Classical and Quantum Formulations”, Physical Review B, vo. 85, no. 16, pp. 165428, 2012.

[16] F. Alibart, L. Gao, B. Hoskins, D.B. Strukov, “High-Precision Tuning of State for Memristive Devices by Adaptable Variation-Tolerant Algorithm”, Nanotechnology, vol. 23, art. 075201, 2012.

[17] Y.N. Joglekar, S.J. Wolf, “The Elusive Memristor: Properties of Basic Electrical Circuits”, arXiv: 0807.3994 v2 [cond-mat.mes-hall] 13 January 2009, pp. 1-24.

[18] J.E. Slotine, W. Li, Applied Nonlinear Control, Prentice Hall, Englewood Cliffs, N.J., 1991.